ELT-ESE-2 DSDL

Digital Systems Design

practical work

HAN Electrical Engineering/Embedded Systems

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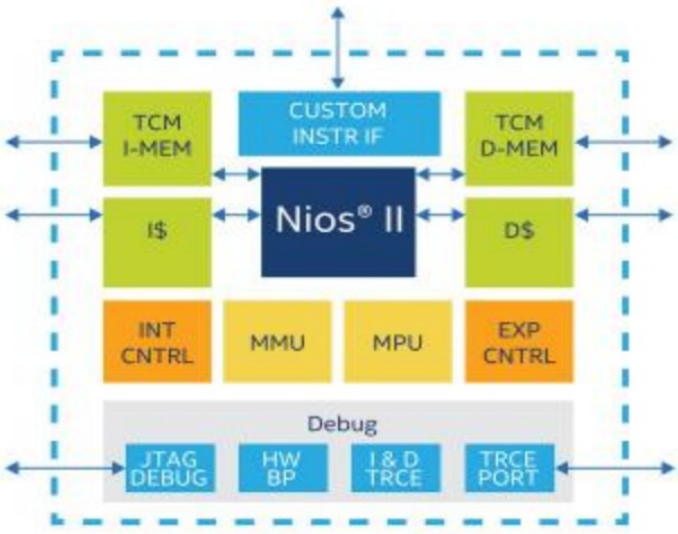
The “grand” assignment: Build a SoftCore in the Altera FPGA



Goal:

The development in five weeks of a working "hello world" application that runs on an Altera Cyclone III / V or MAX10 FPGA. Developing the application leads to a good understanding of how and when a softcore can be used, as well as how the link between the software and the hardware implementation takes place.

Time:

Five weeks.

Required matters and preconditions:

- The workshop has to be executed in couples - alone or with more than two students is not allowed. For odd numbers, only one group may consist of one or three persons.
- Altera Quartus installed on a PC.
- An Altera Cyclone DE0 / DE0-CV / DE10-Lite development board.
- The softcore must be programmed using the language C and / or C ++, the programmable hardware must be written in VHDL.
- The softcore uses the following peripherals:
    - the PIO controller
    - the USART controller
    - [optional, instead of the USART] the VGA controller
- The application (code + data) must be carried out in internal SRAM.

Description:

Design an application that does the following:

- The application starts and waits for a key press.
- After pressing a push button, the application on the seven segment displays shows the scrolling text "HAN ESE DSD 2019-2020 IS COOL". The scroll frequency is 1 Hz.
- Choice of two options:
- The same text is sent simultaneously via the existing UART port with 38400 Baud, 8 Bits, no stop, no parity.
- The same text is displayed on a VGA screen, moving from left to right. When you reach the screen end, the text must move back to the beginning. This implementation results in an extra point for the theory grade.
- When scrolling, an LED on the board must flash along with the scripting frequency.
- The application must be based on a combination of an Altera Nios II softcore with additional VHDL based hardware to perform the tasks that are not or less easily possible in the softcore.

Proceed as follows:

- Get to know the softcore architecture. Watch this Altera video to start.
- Learn the specific softcore tools in Quartus (Qsys / Platform Designer).
- Design the architecture. Divide functionality over softcore and programmable hardware and research how these can be combined in an FPGA project. The link between softcore and programmable hardware is essential in this assignment.
- Divide the tasks. A person provides the sofcore implementation, the other the hardware implementation, separately from each other. Test the two parts separately.
- Add the parts together and test the whole.

Delivery:

You are expected to deliver the following items:

- A working application that meets the purpose described above.
- A small report, containing an explanation of the source code (SW / HW sources) of the embedded application.
- Provide a demonstration of the application to the teacher, or make a video in which you can clearly see that you have written the code and demonstrate that the application works according to the requirements.